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Review article

Performance of Thin Film Transistor: A Review

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ABSTRACT

Transparent electronics becomes one of the most advanced topics for wide range of device applications. The key components are wide band gap semiconductors, where oxides of different origins play an important role as passive component and also as active component, similar to what is observed in conventional semiconductors like silicon. Transparent electronics has gained special attention during the last few years and is today established as one of the most promising technologies for leading the next generation of flat panel display due to its excellent electronic performance. In this paper the recent progress in n-type oxide based thin-film transistors (TFT) is reviewed. After a short introduction where the main advantages of these semiconductors are presented, as well as the industry expectations, the beautiful history of TFTs is revisited. Then, an overview is presented of TCAD simulation tool for TFT.

Keywords: TFT; ZnO; Organic thin film; TCAD

1. Introduction

While microelectronics and now nanoelectronics continue the trend towards smaller and smaller devices, there are also many in the electronics community pushing the idea that "bigger can be better". As revolutionary as microelectronic integrated circuits (ICs) have been, there are functions that are not well addressed by conventional microelectronic IC technology. While the advance of microelectronics and nanoelectronics has tended to make IC devices smaller and smaller, applications that require large-area electronics are difficult or prohibitively expensive to achieve with conventional IC technology. These are the main reasons for the success of thin-film electronics that can be produced at low process temperatures. Thin-film electronics permit solutions that would not be economically viable or even possible with commercial IC microelectronics.

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A TFT is a special kind of Field effect transistor made by depositing thin films of a semiconductor active layer as well as dielectric layer and metallic contacts over a supporting substrate. A common substrate is glass, since the primary application of TFTs is in liquid crystal displays (LCD). This differs from the conventional transistor where substrate is semiconductor material itself, such as a Si wafer. TFTs are used in television sets, computer monitors, mobile phones, personal digital assistants, navigation systems, projectors etc. Fig.1 shows a simple structure of TFT.

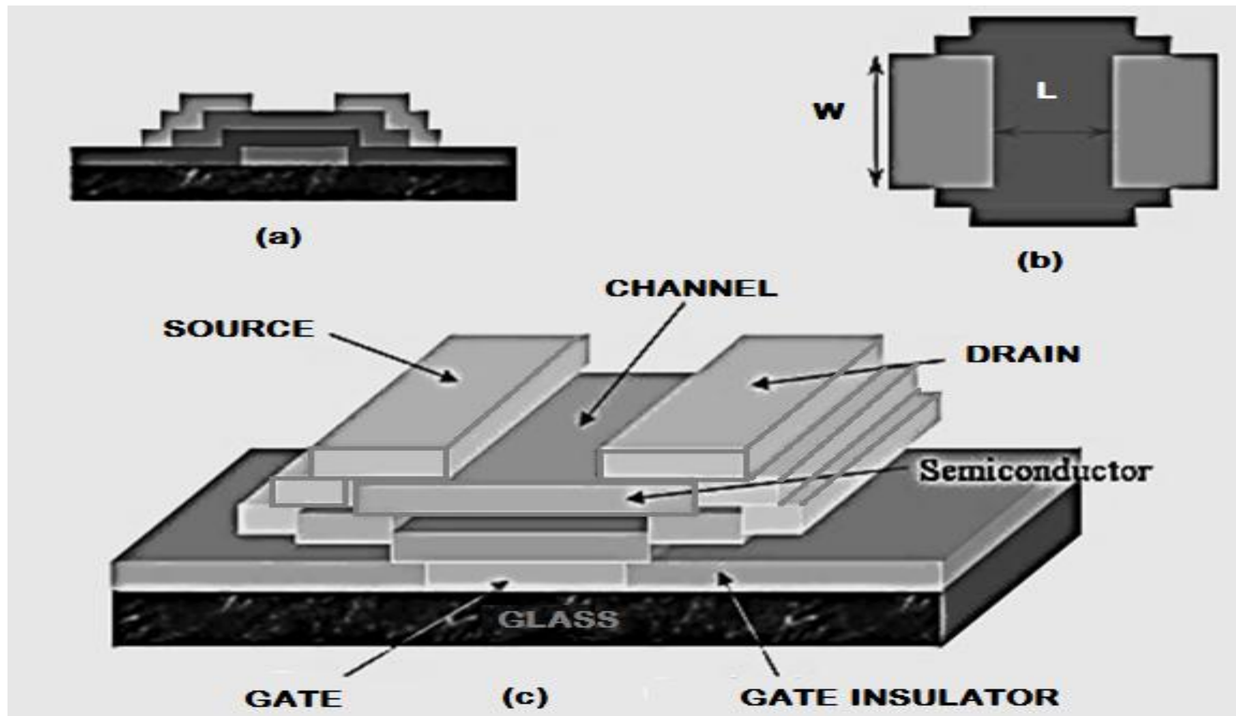

Fig. 1. Basic Thin Film Transistor

Other materials which have been used as semiconductors in TFTs include compound semiconductors such as Cadmium Selinium (CdSe) and metal oxides such as Zinc oxide (ZnO). Over the past several years, the inherent scaling limitations of electron devices have fueled the exploration of high carrier mobility semiconductors as a Si replacement to further enhance the device performance. In particular, compound semiconductors heterogeneously integrated on Si substrates have been actively studied, combining the high mobility of compound semiconductors and the well-established, low cost processing of Si technology.

With the continuous demand in reduction of physical gate lengths of the electronic devices such as TFTs new device architectures will be required to reach the performance of the future technology generation. In addition, control of gate leakage current requires the introduction of gate insulators with high dielectric constants, and the need for increased carrier mobility pushes the use of unconventional channel materials and processing to induce appropriate stresses. The availability of advanced models and simulation tools has significant importance to achieve these goals due to following reasons:

(i) Early evaluations of the most promising device architectures and materials in terms of performance and potential for continued scaling.
(ii) Assessments of processing and design strategies.
(iii) Reductions of cycle time and of R&D costs. Measurements and tests at the nanoscale tend to be much more expensive than at the microscale and macroscale.

Thin-film transistors (TFT's) including an active layer of hydrogenated amorphous silicon (a-Si:H) have been widely employed as the pixel-driving elements of a liquid crystal display (LCD) [1]. When employing a-Si:H layer, the main issues are to increase the field-effect mobility, to reduce the off-state leakage current under backlight illumination and to reduce the bias-stressed change in TFT performance. The improvement in the field-effect mobility of a-Si:H TFT is in particular very important for large-area LCD monitor and TV applications. Recently, several approaches have been carried out to improve the performance of a-Si:H TFT. The surface roughness of silicon nitride (SiN) [2] and hydrogen plasma treatment on the SiN prior to a-Si:H deposition [3] improve the performance. These results indicate that the interface between a-Si:H and SiN is important to improve the TFT performance.

Hydrogenated amorphous silicon thin-film-transistors (a-Si:H TFTs) have presently been the most widely used devices in the active-matrix flat panel display (AM-FPD) due to the low process temperature, uniform device characteristics over large area and low fabrication cost [4]. Recently, the integration of gate drivers with the a-Si:H TFTs on glass substrates has been intensively investigated since it can not only eliminate the external gate driver ICs and the related bonding connections, but also simplify data driver configuration, thereby leading to an overall cost reduction and performance improvement on compactness and reliability, as well as resolution due to the alleviated limitation on pitch size by external connections [5]. However, the a-Si:H TFT is usually difficult to be used for making integrated circuits due to its poor driving ability and severe shift over long operation time [6]. Even though, several integrated a-Si:H gate drivers have been proposed in recent years [7], where, a large size of driving TFT, with the gate voltage bootstrapped during pull-up period is used to promote the circuit speed. And the pull-down TFTs are turned -off every half period by two complementary clocks to suppress shift.

TFTs made of metal-oxide-semiconductors over the last several years [8]. This is mainly due to unique advantages of metal-oxide-semiconductor TFTs, such as visible light transparency, large-area uniform deposition at low temperature, and high carrier mobility. However, conventional metal-oxide- semiconductors based on zinc oxide (ZnO) are polycrystalline in nature, even at room temperature (RT). The grain boundaries of such metal oxides could affect device properties, uniformity, and stability over large areas. To overcome this issue, a new ternary oxide material composed of In, Ga, Zn, and O has been proposed as a channel layer in TFTs [9]. The amorphous indium-gallium-zinc-oxide (a-IGZO) thin film can more easily form a uniform amorphous phase while maintaining high carrier mobility like most oxide semiconductors. Therefore, a-IGZO TFTs have emerged as one of the promising candidates substituting a-Si:H, LTPS, and organic TFTs as switching/ driving devices in AMLCDs and/or AMOLED displays.

Oxide semiconductor material has attracted increased attention because of the two characteristics that it exhibits in the visible light region: optical transparency and electrical conductivity. In particular, in recent years, indium tin oxide (ITO) known for its good transparency and conductivity has been used widely as a transparent electrode material for solar cells and displays. The material is thus becoming more and more common in our daily lives. However, the attention has been limited to its transparency and conductivity and its potential as a functional material for semiconductor devices is yet to be considered. Under such circumstances, Professor Hideo Hosono of the Tokyo Institute of Technology et al. released, in sequence, a monocrystal transparent oxide transistor using $InGaO_3$ $(ZnO)_5$ in 2003 and a thin film transistor (TFT) deposited at room temperature with an amorphous $InGaZnO_4$ phase in 2004 [10]. In particular, Japanese, Koreans and Taiwanese panel manufacturers have been playing leading roles in vigorous trial manufacture of large displays. After much discussion about reliability and stability, and with some advanced consideration of issues relating to mass production, the technology has nearly reached a practical level [11]. Among such TFTs are ZnO [12], Zn-Sn-O and In-Zn-O [13], reported mainly by Oregon State University. Today, the number of those reported cases has been increasing dramatically. In addition, at SID [14], Those are the issues yet to be overcome for the future, and there has already been a fierce competition among research institutes from a technical perspective of how to realize high-mobility and stable elements even in a low-temperature process [15]. The current deposition techniques for highquality GaN-related thin films are mainly metal-organic chemical vapor deposition and molecular beam epitaxy. One of the current directions in GaN research is to deposit high-quality GaN thin films using inexpensive substrate under low temperature. Recently, amorphous and polycrystalline GaN thin films have been deposited using the magnetron sputtering technique [16] or the pulsed laser deposition technique [17]. The dc magnetron sputtering technique for the thin-film deposition has the potential of high deposition rate, large area, good uniformity, and low cost, suitable for mass production in the industry. Transparent amorphous indium-gallium-zinc oxide thinfilm transistors (TFTs) have become attractive for use as driving devices in large-scale active-matrix organic light-emitting diode applications, due to their higher mobility and larger area uniformity, as compared with amorphous and polycrystalline silicon TFTs [18]. However, the poor electrical stability of ZnO-based TFTs is still a main issue in preventing commercialization [19].

Gallium nitride has emerged as one of the most promising compound semiconductor during the last few years [20]. GaN-based high-electron mobility transistors are the focus of intense research activities in the area of highpower, high-speed, and high-temperature transistors [21]. The current deposition techniques for high-quality GaN-related thin films are mainly metal-organic chemical vapor deposition (CVD) and molecular beam epitaxy.

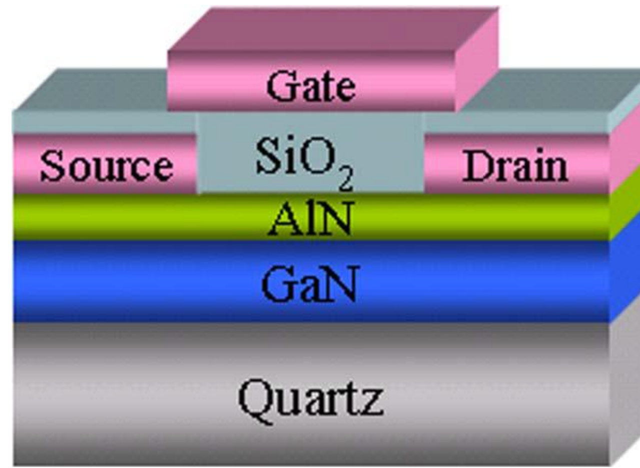

Fig. 2. Schematic of the proposed GaN TFT with a top-gate structure.

One of the current directions in GaN research is to deposit high-quality GaN thin films using an inexpensive substrate under low temperature. Recently, amorphous and polycrystalline GaN thin films have been deposited using the magnetron sputtering technique [22] or the pulsed laser deposition technique [23]. The dc magnetron sputtering technique for the thin-film deposition has the potential of high deposition rate, large area, good uniformity, and low cost suitable for mass production in industry.

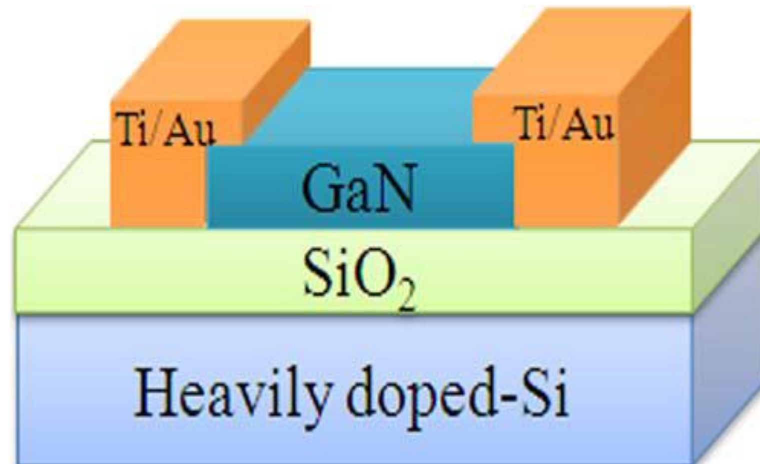

Fig. 3. Cross-sectional schematic of the proposed GaN TFT with a bottom gate structure.

The Thin-film transistor (TFT) is the basic building block of “large area electronics,” a name given to describe electronic devices or circuits distributed over large areas of a substrate. Typically, the substrate is made of glass or plastic. Applications of large area electronics include the addressing and drive pixel circuitry in active matrix displays, X-ray imagers, and large area sensors [24]. As the field develops there is a need for more advanced devices and circuits that can, for example, add functionality [25], correct for variations in transistor performance, or compensate at a pixel level for device aging [26]. The TFT is a member of the family of field-effect transistors (FETs) [27]. They all operate in the same way: a voltage applied to the gate

modulates the conductance between a source and drain electrode. Ideally, the source and drain contacts to the channel are ohmic. Saturation of the drain current occurs when the drain voltage reaches a voltage where the channel at the drain end is depleted of free carriers and is pinched off [28].

Flexible electronics are becoming increasingly important because of the advantages of flexibility, thin form factor, and light weight. In particular, the roll-to-roll process technology using flexible substrates is the most attractive because of its high-throughput capability and, thereby, very low manufacturing cost [29]. However, the device characteristics of low-temperature organic and a-Si thin-film transistors (TFTs) on flexible substrates of low glass transition temperature are insufficient to meet the requirements of active devices for high-performance applications. Recently, low-temperature amorphous indium-gallium-zinc oxides (a-IGZO) TFTs have attracted much attention for applications on next-generation displays and flexible electronics, owing to their high mobility and transparency [30]. Although excellent electrical characteristics have been shown in previous studies [31,32], a-IGZO TFTs often require thermal annealing after device fabrication. The development of a-IGZO TFTs compatible with a roomtemperature roll-to-roll process is less addressed.

Amorphous In-Ga-Zn-O (α-IGZO) thin-film transistors (TFTs) are promising as next-generation electronic devices because they are transparent, exhibit high performances, and can be fabricated on plastic substrates at low temperatures [33]. Therefore, α-IGZO TFTs have been extensively developed for flat-panel displays such as active-matrix liquid-crystal displays [34] active-matrix organic light-emitting diode displays [35] and electronic papers [36]. Recently, we have found that a-IGZO TFT exposed to ozone annealing at 300^0C has an interesting property [37]. The Ids-Vgs characteristic shifts positively, and the subthreshold slope becomes steep when the gate bias is applied, whereas the Ids-Vgs characteristic shifts negatively and the subthreshold slope becomes gradual when the light is irradiated. This is because excess oxygen generates flat trap states around the Fermi level in the energy gap, and the trap states descend to deeper Gaussian-like states owing to the structural relaxation of the charged states and behave as negative fixed charges when the gate bias is applied, whereas the trap states return to the flat states owing to the carrier detrapping by the photoexcitation when the light is irradiated, which is written in detail in a prior paper [37].

During the past few years, ZnO has attracted much attention as a channel material of thin-film transistors (TFTs) for the application in the field of flat-panel displays (FPDs) due to its superior properties including wide direct band gap, high carrier mobility and transparency in the visible range [38]. Nevertheless, it is very difficult to form amorphous or singlecrystalline ZnO thin films, and in general a polycrystalline structure is obtained, resulting in grain-boundary defects. Accordingly, the uniformity of device performance at different locations across a single FPD can be deteriorated. In addition, the poor chemical durability of pure ZnO against acidic etchants is another drawback of this material, increasing the difficulty in fabrication [39]. Aiming to solve these problems, amorphous InGaZnO (a-IGZO) has been developed to replace ZnO as the channel material in TFTs [40]. Recently, various high-k materials have been adopted

as the gate dielectrics of a-IGZO TFTs in order to reduce their operating voltage. Among them, Ta_2O_5 has been regarded as one of the most promising candidates due to its high dielectric constant, large refractive index and excellent step coverage [41].

This plasma-enhanced crystallization can also be spatially controlled by masking with patterned silicon oxide or silicon nitride, so that both amorphous and polycrystalline areas can be realized simultaneously at desired locations [42,43]. Integration of -Si:H and poly-Si TFTs is traditionally difficult for three reasons. First, the conventional -Si:H TFT fabrication process is a low-temperature process (350^0C) [44], while the poly-Si TFT fabrication requires a 500-600^0C crystallization anneal to form the polycrystalline layer, if no laser processing is involved. Second, one would like to deposit only a single Si layer instead of two (a-Si:H and poly-Si) to save cost. Third, the structure and fabrication sequence of -Si:H TFTs and poly-Si TFTs are quite different (e.g., bottom gate versus top gate process), so that few process steps can be shared. Various techniques have been tried to integrate -Si:H and poly-Si TFTs on the same substrate. One method is excimer laser annealing to crystallize the chemical vapor deposited (CVD) deposited a-Si selectively and fabricate bottom gate transistors in both the amorphous and polycrystalline regions [43]. Another method uses crystallization of a thin (20 nm) -Si :H layer deposited by plasma-enhanced CVD (PECVD) using Ar and XeCl (300 mJ/cm), and subsequent deposition of a thick (200 nm) -Si :H layer and patterning the -Si :H to realize staggered layers of poly-Si and -Si :H. Top gate TFTs were then fabricated in the two regions [45]. Both of these methods involve laser processing, which has relatively low throughput and also can lead to variable film quality due to variations in laser beam power and width. Also, the latter method involves fabrication of TFTs in staggered layers, i.e., the transistors are not in a single silicon layer.

Zinc oxide (ZnO), an important semiconductor material, has received much attention over the past few years owing to its direct wide band gap ($Eg \approx 3.37$ eV) and relatively large binding energy (60 meV) at room temperature [46]. It is also a very crucial versatile material with wide ranging applications such as the blue to ultraviolet (UV) light-emitting diodes (LEDs), piezoelectric devices, sensors in MENS-based devices, transparent electrodes, flexible displays, solar cells, gas sensor devices, piezoelectric devices, and so on. In recent years, the technology of flat-panel displays thin-film transistor light-emitting diode (TFT-LED) has played an important role in our daily lives, because that TFT-LED has the advantages of thin lightweight, low-radiation, low-power and long life-time. ZnO has attracted considerable attention as a high performance device in TFT manufacturing field due to ZnO possessing many interesting characteristics such as piezoelectric, ferroelectric properties and n-type conductivity. ZnO thin film transistors (TFTs) present an attractive alternative to amorphous Si TFTs because of their high mobility with value greater than 10 cm2/V-s and low process temperature ($<250^0$) [47]. Meanwhile, ZnO TFT has low-cost and large size backplane for active-matrix organic light-emitting diode (AMOLED). Conventional AMOLED displays suffer from the non-uniformity of their mobility and threshold voltage owning to the existence of gain boundaries. Consequently, the development of amorphous ZnO TFTs is essential and critical for the fabrication of

competitive AMOLED. Many studies have been carried out and various deposition techniques, such as physical vapor deposition (PVD), radio frequency (RF) sputtering, molecular beam epitaxy (MBE) and metal organic chemical vapor deposition (MOCVD), have been widely investigated to deposit ZnO thin films [48]. Until now, the main processes to deposit crystalline ZnO layers for thin-film transistors (TFTs) include (1) vacuum-based deposition, such as radiofrequency magnetron sputtering, ion beam sputtering, and pulsed laser deposition, (2) gas phasebased deposition, such as chemical vapor deposition and atomic layer deposition, and (3) solution-based deposition, such as chemical bath deposition and sol-gel processes. However, vacuum-deposition method has some shortcomings that makes itself could not be compatible with low-cost TFT manufacturing processes due to expensive equipment, high energy consumption and low throughput. Gas phase-based depositions generally involve complex and high-temperature process, high cost and time-consuming controlling steps. Solution-processed thin-film deposition methods can offer many advantages such as simplicity, low cost, and high throughput that enable the fabrication of high-performance and low-cost electronics [49]. Therefore, solution-processed thin-films semiconductors can potentially enable low-cost TFT manufacturing for vast electronic applications of immense commercial implications as they can be deposited/patterned using conventional low-cost solution techniques.

During the past few years, amorphous InGaZnO (a-IGZO) thin-film transistors (TFTs) have attracted much attention for the application in various flat-panel displays, including electronic paper, active-matrix organic light-emitting diode display and active-matrix liquid-crystal display [50]. Compared to conventional amorphous silicon or organic TFTs with a field-effect carrier mobility of ~1 $cm^2/V \cdot s$ [120], a- IGZO TFTs typically exhibit a mobility higher than 10 $cm^2/V \cdot s$ [51], which an help realize higher switching speed for electronic devices. Moreover, a-IGZO TFTs can offer better uniformity in device characteristics than polycrystalline silicon TFTs [52]. Besides, a-IGZO TFTs, with a wider-bandgap semiconductor material, have better transparency to visible light than all the silicon-based devices. In order to achieve smaller threshold voltage (V_{TH}) and higher on-current, various high-k materials have been adopted as gate dielectric in TFTs.

The indium-gallium-zinc oxide (IGZO) thinfilm transistor (TFT) has shown high potential to provide large drive current, especially required for driving high-resolution light-emitting diode. The amorphous IGZO TFTs give several advantages over poly-silicon TFT including high mobility and low-thermal budget for TFT process, which offer highly integrated capability with high-resolution flexible display. Although various high-κ gate dielectrics are proposed [53], for low-temperature flexible TFT fabrication, they cannot overcome the defect issues including low dielectric constant (κ value) and high-intrinsic leakage, even using commercial HfO2 (κ ~16) and ZrO2 (κ ~18) dielectrics [54]. In addition to large operating voltage, IGZO flexible TFTs still suffer from high subthreshold swing (SS) and low-device mobility that is most critical for high-speed and high-resolution display application. To investigate these issues on low-temperature flexible device, we fabricate a high-performance α-IGZO TFT using high-κ $SiO_2/TiO_2/SiO_2$ (STS) dielectric on polycarbonate (PC) substrate at room temperature (RT). The

high-κ TiO_2 has a very high-κ value of > 40, which can benefit the driving current and lower down the operating voltage. This flexible IGZO TFT shows a small SS of 0.129 V/decade, a low threshold voltage (V_t) of 0.5 V and a high field effect mobility (μFE) of 76 cm2 /Vs, which is much better than other reported low-temperature (or RT) TFT devices [53].

Amorphous indium-gallium-zinc-oxide thin-film transistors (a-IGZO TFTs) have been considered as a very serious candidate for high-resolution large-area active-matrix flat-panel displays (AM-FPDs) [54]. This is due to their high field-effect mobility μEFF, low leakage current *I*OFF, good electrical stability, superior optoelectronic characteristics, and low temperature fabrication [119]. It is well known that the electrical performance of metal-oxide-semiconductor field-effect transistors (MOSFETs) is improved when a larger portion of the channel area is controlled by an additional gate electrode [55]. Dual-gate (DG) amorphous silicon (a-Si:H) TFTs have also been proposed to provide effective light shielding to prevent the degradation of the TFT's electrical properties under illumination [56]. However, the presence of bias on the additional gate electrode introduces unwanted increases in the a-Si:H TFT's subthreshold swing (SS) and off current *I*OFF. To address this problem, the additional gate electrode has been grounded to provide stable circuit operation in a pixel array [57]. Several results on DG a-IGZO TFTs have recently been reported [58].

Organic thin-film transistors (OTFTs) have been the focus of considerable research for their potential applications, such as display driver logic, sensors and low-cost electronic circuits. The low cost and the compatibility with flexible substrate are two of the most important advantages. Although there has been tremendous progress in the research of OTFTs over the last two decades, only a few attempts have been made to link the nonvolatile memory with the OTFT, which at present is mainly achieved by using ferroelectric materials, such as $PbZrTiO_3$ [62], or electret polyvinyl alcohol [59] as the gate insulating layer. The direction of the polarization of the gate dielectric layer modulates the channel conductance. Another way to make a TFT memory is by using a floating gate structure, where a floating gate is generally intro- duced into the gate dielectric. This approach has seen dramatic progress in the field of silicon-based nonvolatile memory. However, the attempt of the floating gate TFT memory based on organic semiconductors is rarely reported [60].

Organic thin-film transistors (OTFTs) have enormous market potential in a wide range of applications; these include flexible displays and radio-frequency identification tags [61]. Many studies have reported on the characterization and modeling of the electrical properties of OTFTs [62], mainly for dc behavior, but a few studies have reported on ac characteristics. Recent works [63], have reported that an organic circuit may be capable of operating at only a few kilohertz due to limited carrier mobility in the organic active layers. Miyadera et al. [62] measured the capacitance-voltage characteristics of a pentacene TFT and reported a cutoff frequency at several tens of kilohertz but did not provide intrinsic capacitances, such as CGD and CGS, which are essential for OTFT circuit simulation. For accurate estimation of the dynamic behavior of organic circuits, extraction of a small-signal capacitance on each terminal is critically required.

2. Simulation of TFT Using Sentaurus TCAD Tool

Value of Sentaurus TCAD in Technology Development and Optimization

Semiconductor manufacturers face the challenge of developing process technologies within strict time and cost constraints. One key factor impacting development time and cost is the number of engineering wafers needed to complete the development of the new process. By simulating the process flow and device operation before any wafers are processed and during wafer-based process optimization, TCAD reduces the number of engineering wafers, saving time and money. Morever, Sentaurus TCAD simulations provide engineers with important insights on the behavior of semiconductor devices which can lead to new device concepts.

2.1 Sentaurus Process

Simulator Sentaurus Process simulates the fabrication steps in silicon process technologies in 2-D and 3-D. Equipped with a set of advanced process models, which include default parameters calibrated with data from equipment vendors, Sentaurus Process provides a predictive framework to simulate a broad spectrum of technologies, ranging from nanoscale CMOS to high-voltage power devices.

2.2 Sentaurus Structure Editor

Sentaurus Structure Editor is a 2-D/3-D device editor which builds and edits device structures using geometric operations. Sentaurus Structure Editor is powered by the ACIS® geometry kernel, which is well proven and widely used in many CAD applications.

2.3 Sentaurus Device

Sentaurus Device simulates the electrical, thermal, and optical characteristics of silicon and compound semiconductor devices in 2-D and 3-D. Sentaurus Device supports the design and optimization of current and future semiconductor technologies including nanoscale CMOS, FinFET, thin film transistors (TFTs), flash memory, SiGe heterojunction bipolar transistors (HBTs), large-scale power devices, compound semiconductors, CMOS image sensors, and solar cells. Sentaurus Device has an extensive set of models and parameters to support compound semiconductor device development, including spatially varying mole fractions, heterointerfaces, bulk and surface trapping, polarization effects in GaN, anisotropic effects in SiC, and spatial quantization in 2-D electron gases.

2.4 Sentaurus Visual TCAD Visualization

Sentaurus Visual provides users with a state-of-the-art interactive 1-D, 2-D, and 3-D visualization and data exploration environment. Sentaurus Visual supports TCL scripting, enabling the postprocessing of output data to generate new curves and extracted parameters.

3. Conclusions

In the present study, although several literatures on polycrystalline compound semiconductors and metal oxide is available, influence of all the material parameter on the TFT characteristics is not clearly understood. Hence in an attempt to study the effect of compound semiconductor material parameters, temperature, substrate used and other possible factors that can have effect on the performance of TFTs. The TCAD (Technology CAD) simulation tool will be used in the present work. It is expected that TCAD tool will be helpful for gaining insight in the field effect physics of Compound semiconductors TFTs.

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